



Docket No. BUR920010100US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Joseph A. Iadanza

Group Art Unit: 2815

Filed: 2/26/2002

Examiner: Ortiz, Edgardo

Serial No.: 09/683,872

Title: **METHOD OF CONNECTING CORE I/O PINS TO BACKSIDE CHIP I/O PADS**

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**RESTRICTION ELECTION**

In response to the Restriction Requirement dated October 2, 2003, Applicant hereby provisionally elects Group I, claims 1-16, drawn to an integrated circuit, classified in class 257, subclass 725. This election is made with traverse, and Applicant hereby reserves the right to file a divisional application in connection with unelected claims 17-22, drawn to an electronic device.

With regard to the Restriction Requirement, Applicant respectfully submits that the subject matter of all claims 1-22 is sufficiently related that a thorough search for the subject matter of any one group of claims would encompass a search for the subject matter of the remaining claims. Thus, Applicant respectfully submits that the search and the examination of the entire application could be made without serious burden. See MPEP § 803, in which it is stated that "if the search and examination of the entire application can be made without serious burden, the Examiner must examine it on the merits (emphasis added)." Applicant respectfully submits

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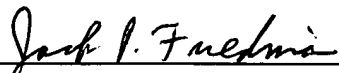
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09/683,872

that this policy should apply in the present application in order to avoid unnecessary delay and expense to Applicant and duplicative examination by the Patent Office.

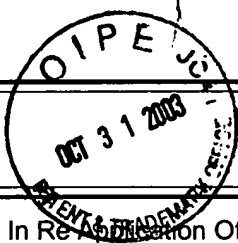
Should the Examiner require or request anything further from Applicant prior to examination, the Examiner is requested to contact Applicants' undersigned representative at the telephone number below. Otherwise, Applicant requests early and favorable examination on the merits.

Date: 10/29/2003

  
\_\_\_\_\_  
Jack P. Friedman  
Registration No. 44,688

Schmeiser, Olsen & Watts  
3 Lear Jet Lane, Suite 201  
Latham, New York 12110  
(518) 220-1850

2815



**TRANSMITTAL LETTER**  
**(General - Patent Pending)**

Docket No.  
**BUR920010100US1**

In Re Application Of: **Jospeh A. Iadanza**

# 3/Electronic  
asn  
11/6/03

Serial No. <b>09/683,872</b>	Filing Date <b>2/26/2002</b>	Examiner <b>Ortiz, Edgardo</b>	Group Art Unit <b>2815</b>
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Title: **METHOD OF CONNECTING CORE I/O PINS TO BACKSIDE CHIP I/O PADS**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is:

**Response to Restriction**

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of \_\_\_\_\_ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456(IBM)** as described below.
  - ☐ Charge the amount of \_\_\_\_\_
  - ☒ Credit any overpayment.
  - ☒ Charge any additional fee required.

  
\_\_\_\_\_  
Signature

Dated: **10/29/2003**


**Jack P. Friedman**  
**Reg. No. 44,688**  
**Schmeiser, Olsen & Watts**  
**3 Lear Jet Lane, Suite 201**  
**Latham, NY 12110**  
**(518) 220-1850**

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CC:

I certify that this document and fee is being deposited on <b>10/29/2003</b> with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
 _____ Signature of Person Mailing Correspondence	
<b>Kim Dwileski</b> _____ Typed or Printed Name of Person Mailing Correspondence	